Amendments to the Claims

The following Listing of Claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-38 (canceled)

Claim 39 (currently amended): An integrated circuit comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation structure ~~layer~~ having at least one contact via extending therethrough;

a ferroelectric device level positioned over the transistor isolation layer, the ferroelectric device level completely encompassing ~~including~~ at least one ferroelectric capacitor structure comprising a top electrode having an electrical contact area, a bottom electrode and ferroelectric dielectric material disposed between the top and bottom electrodes, the ferroelectric device level further including a ~~and an overlying~~ ferroelectric isolation ~~layer~~ structure disposed over at least a portion of the top electrode of the at least one ferroelectric capacitor structure and electrically isolating non-electrical contact areas of the at least one ferroelectric capacitor structure from overlying and adjacent electrical structures, the ferroelectric isolation structure having at least one via extending therethrough and aligned with a corresponding contact via of the transistor isolation layer, the at least one via extending through the ferroelectric isolation structure ~~layer~~ being laterally sized larger than the corresponding contact via of the transistor isolation structure aligned therewith;

a first wiring ~~metal~~ level disposed over the ferroelectric device level;

an inter-level dielectric level disposed over the first wiring ~~metal~~ level; and

a second wiring ~~metal~~ level disposed over the inter-level dielectric level.

Claim 40 (previously presented): An integrated circuit, as defined in claim 39, wherein each contact via is filled with a respective tungsten contact plug.

Claim 41 (currently amended): An integrated circuit, as defined in claim 40, wherein each ferroelectric capacitor structure is formed over a respective tungsten contact plug.

Claims 42-56 (canceled)

Claim 57 (currently amended): A method of forming an integrated comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation structure ~~layer~~ having at least one contact via extending therethrough;

forming a ferroelectric device level over the transistor isolation layer, the ferroelectric device level completely encompassing ~~including~~ at least one ferroelectric capacitor structure comprising a top electrode having an electrical contact area, a bottom electrode and ferroelectric dielectric material disposed between the top and bottom electrodes, the ferroelectric device level further including a ~~and an overlying~~ ferroelectric isolation ~~layer~~ structure disposed over at least a portion of the top electrode of the at least one ferroelectric capacitor structure and electrically isolating non-electrical contact areas of the at least one ferroelectric capacitor structure from overlying and adjacent electrical structures, the ferroelectric isolation structure having at least one via extending therethrough and aligned with a corresponding contact via of the transistor isolation layer, the at least one via extending through the ferroelectric isolation structure ~~layer~~ being laterally sized larger than the corresponding contact via of the transistor isolation structure aligned therewith;

forming a first wiring ~~metal~~ level over the ferroelectric device level;

forming an inter-level dielectric level over the first wiring ~~metal~~ level; and

forming a second wiring ~~metal~~ level over the inter-level dielectric level.

Claim 58 (previously presented): A method of forming an integrated circuit, as defined in claim 57, wherein each contact via is filled with a respective tungsten contact plug.

Claim 59 (previously presented): A method of forming an integrated circuit, as defined in claim 58, wherein the ferroelectric capacitor is formed over a respective tungsten contact plug.

Claim 71 (previously presented): An integrated circuit, as defined in claim 39, wherein between the ferroelectric device level and the transistor isolation layer is free of any interposing wiring ~~metal~~ level.

Claim 72 (currently amended): An integrated circuit, as defined in claim 39, wherein throughout the ferroelectric isolation structure the at least one via extending therethrough ~~layer each ferroelectric isolation layer via~~ is laterally sized larger than the corresponding contact via of the transistor isolation structure.

Claim 73 (previously presented): A method of forming an integrated circuit, as defined in claim 57, wherein between the ferroelectric device level and the transistor isolation layer is free of any interposing wiring ~~metal~~ level.

Claim 74 (previously presented): A method of forming an integrated circuit, as defined in claim 57, wherein throughout the ferroelectric isolation structure the at least one via extending therethrough ~~layer each ferroelectric isolation layer via~~ is laterally sized larger than the corresponding contact via of the transistor isolation structure.